



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,391	08/29/2001	Richard W. Busser	4430-26	9713
22442	7590	12/03/2004	EXAMINER	
SHERIDAN ROSS PC 1560 BROADWAY SUITE 1200 DENVER, CO 80202				CHOI, WOO H
		ART UNIT		PAPER NUMBER
		2186		

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,391	BUSSER ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 September 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benhase *et al.* (US Patent No. 6,665,743, hereinafter “Benhase”) in view of Hansen *et al.* (US Patent No. 6,697,913, hereinafter “Hansen”)

3. With respect to claims 1, 18 and 20, Benhase discloses a method for initializing an array of drives, comprising:

providing an array of drives (figure 1) including a first drive and a second drive (4), a controller (6) and a bus subsystem that enables communications between said controller and said array of drives (col. 6, lines 56 – 57, SCSI), each of said drives being associated with a priority and with said first drive having greater priority than said second drive (according to the specification, SCSI devices has a SCSI identifier with an assigned priority, see specification page 2, lines 12 – 14); and

causing substantially equal usage of said bus subsystem by all of said drives while performing a zero initialization of said drives (figure 3, zero initialization occurs one stripe at a time, i.e. one block per disk drive resulting in a substantially equal usage of the bus),

wherein said causing substantially equal usage of said bus subsystem includes:
issuing a first number of write operations to each of said drives in said array (figure 3,
114 – 130), wherein each of said first number of write related operations issued to a one of said
drives concerns a different logical block address (col. 3, lines 1 – 5, line 15) range than any other
of said first number of write related operations issued to said one of said drives (write operation
for sector 2 concerns address range 0 – 2, and for sector 4 concerns a an address range 0 – 4, or 3
– 4 which are different from ranges 0 – 2 and 1 – 2).

However, Benhase does not specifically disclose that the method issues at least one more
write related operations in response to determining whether a write operation has been completed
and that the write related operations are queued. On the other hand, Hansen discloses such a
step. Hansen discloses a method of queuing disk commands wherein a disk operation is issued
in response to determining whether a write operation has been completed (col. 1, lines 48 – 51).

It would have been obvious to one of ordinary skill in the art, having the teachings of
Banhase and Hansen before him at the time the invention was made, to use the command
queuing teachings of the disk storage system of Hansen in the disk storage system of Banhase, in
order to increase the I/O performance of disk drives (Hansen, col. 1, lines 46 – 48).

4. With respect to claims 9 and 12, Benhase discloses an apparatus for initializing an array
of drives (figure 1), comprising:

an array of drives for storing information (4), said array of drives including at least a first drive and a second drive with said first drive being associated with a higher priority than said second drive (col. 6, lines 56 – 57);

a bus subsystem connected to said array of drives (col. 6, lines 56 – 57); and

a controller (6) in communication with said array of drives using said bus subsystem, said controller for controlling issuance of write operations, including a first write operation, second write operation, and a third write operation to said array of drives in order to initialize said drives, wherein said controller controls said first write operation to at least each of said first and second drives, controls said second write operation to at least said first and second drives, and controls said third write operation to at least said first and second drives, and in which said third write operation is controlled to said at least first and second drives after at least one of said first write operation and second operation has been completed on at least each of said second drive and said first drive (figure 3, zero initialization occurs one stripe at a time, so a second stripe is written after the first stripe and a third stripe after the second stripe). The Examiner notes that based on Benhase's disclosure in col. 2, line 52 – col. 3, line 5, one of ordinary skill in the art can immediately discern that an Enterprise Storage Server that takes up to several hours to initialize has a capacity of at least three 524 byte sectors (i.e. at least 3 write operations for initialization).

However, Benhase does not specifically disclose that each drive is associated with a queue. On the other hand, Hansen discloses such a queue (figure 2, 33).

It would have been obvious to one of ordinary skill in the art, having the teachings of Banhase and Hansen before him at the time the invention was made, to use the command queuing teachings of the disk storage system of Hansen in the disk storage system of Banhase, in order to increase the I/O performance of disk drives (Hansen, col. 1, lines 46 – 48).

5. With respect to claims 2 and 11, said causing step includes providing write operations to all said drives of said array during substantially all the time said zero initialization of said drives is being performed (col. 4, line 66 – col. 5, line 3).
6. With respect to claim 3, said causing step includes controlling utilization of said bus subsystem independently of said priority (the bus is utilized substantially equally and independent of the priority arrangement of the SCSI bus since one block is written to every disk per stripe).
7. With respect to claim 4, said issuing a first number of write related operations to each of said drives step includes issuing a predetermined number of at least two write operations to said first drive and a predetermined number of at least two write operations to said second drive and in which subsequent issuing of another write operation to said first drive is made after at least one of said predetermined number of at least two write operations is completed by said second drive and after at least one of said predetermined number of at least two write operations is completed by said first drive (as discussed above, zero initialization occurs one stripe at a time,

i.e. second stripe is written after the completion of the write operation of the first stripe and there are at least three stripes or sectors per disk).

8. With respect to claims 5 and 13, said predetermined number of at least two write operations issued to said first drive relates to one or more ranges of logical block addresses (LBAs) (the write operations to sectors relate to LBA as each sector has an LBA associated with it).

9. With respect to claims 6 and 14, said predetermined number of at least two write operations is four (as discussed above in the rejection of claim 1, Banhase discloses a disk system with at least four sectors, hence at least four writes for initialization).

10. With respect to claims 7, 8, 15 and 16, said causing step includes checking whether a write operation for at least one of said one or more ranges of LBAs has been completed to each of said drives of said array, and issuing a write operation for a next one or more LBA ranges to be written to each of said drives of said array (figure 3, as discussed above, the write operation is done one stripe at a time, i.e.).

11. With respect to claim 10, said bus subsystem is shared substantially equally by all said drives of said array when said controller controls said first: and second write operations (see rejection of claim 1 above).

Art Unit: 2186

12. With respect to claim 17, see rejections of claim 1 and 9 above.

13. With respect to claim 19, as discussed in the rejection of claim 1, Banhase discloses a disk storage system that requires at least five write operations and each write operation is concerns an address range.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
whc

November 19, 2004



MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100